

PTO/SB/08A (02-03)

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet 1 of 3**Complete if Known**

Application Number	10/644,718
Filing Date	08/20/2003
First Named Inventor	Yi-Hsun Wu
Art Unit	2858
Examiner Name	Not Yet Assigned
Attorney Docket Number	N1085-00191

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
DN	AA	US- 3,947,778	03-30-1976	Hsiao	
	AB	US- 5,179,297	01-12-1993	Hsueh et al.	
	AC	US- 5,304,867	04-19-1994	Morris	
	AD	US- 5,381,062	01-10-1995	Morris	
	AE	US- 5,418,476	05-23-1995	Strauss	
	AF	US- 5,504,450	04-02-1996	McPartland	
	AG	US- 5,548,241	08-20-1996	McClure	
	AH	US- 5,576,656	11-19-1996	McClure	
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	AJ	US- 5,589,794	12-31-1996	McClure	
	AK	US- 5,594,373	01-14-1997	McClure	
	AL	US- 5,596,297	01-21-1997	McClure et al.	
	AM	US- 5,598,122	01-28-1997	McClure	
	AN	US- 5,663,917	09-02-1997	Oka et al.	
	AO	US- 5,808,480	09-15-1998	Morris	
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	AR	US- 5,933,027	08-03-1999	Morris et al.	
DN	AS	US- 5,952,848	09-14-1999	Morris	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ Number ⁴ Kind Code ⁵ (if known)				

Examiner
Signature

/Danny Nguyen/

Date
Considered

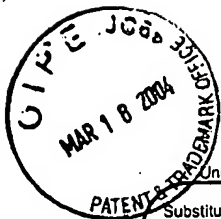
10/24/2006

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Attorney Docket Number	N1085-00191

Sheet	3	of	3
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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
DN	BA	M. Pelgrom and E. Dijkmans, "A 3/5V compatible I/O Buffer," IEEE Journal of Solid-State Circuits, vol. 30, No. 7, Jul. 1995, p.p. 823-825.	
DN	BB	N. Otsuka and M. A. Horowitz, "Circuit Techniques for 1.5-V Power Supply Flash Memory", IEEE Journal of Solid-State Circuits, Vol. 32, No. 8, Aug. 1997, p.p. 1217-1230	
DN	BC	G. Singh and R. Salem, "High-Voltage-Tolerant I/O Buffers with Low-Voltage CMOS Process," IEEE Journal of Solid-State Circuits, vol. 34, No. 11, Nov. 1999, p.p. 1512-1525.	
DN	BD	L. T. Clark, "A High-Voltage Output Buffer Fabricated on a 2V CMOS Technology," 1999 Symposium on VLSI Circuits Digest of Technical Papers, p.p. 61-62.	

Examiner Signature	/Danny Nguyen/	Date Considered	10/24/2006
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